What is claimed is:

1. A testing apparatus for determining the etch bias associated with a semiconductor-processing step, comprising:

a substrate;

a first cathode finger with a first width on said substrate;

a second cathode finger with a second width on the substrate; and

a cathode platform on the substrate;

wherein said cathode platform has a third width W'' and a length L'' that are both substantially larger than either of the first and second widths.

2. The apparatus of claim 1, wherein the width W'' and the length L'' of cathode platform is defined by:

$$\frac{C_{AT}(L''-\Delta)(W''-\Delta)}{2C_{PT}(L''+W''-2\Delta)} > 50,$$

with C_{AT} the theoretical unit area capacitance, C_{AT} the theoretical unit perimeter capacitance, and Δ the etch bias of the cathode platform.

3. The apparatus of claim 1, further comprising:

a first anode finger spaced adjacent to the first cathode finger;

a second anode finger spaced adjacent to the second cathode finger;

wherein the capacitance between the first anode and first cathode fingers is different than the capacitance between the second anode and second cathode fingers.

4. The apparatus of claim 1, wherein the first cathode finger comprises:

a cathode layer;

a cathode ohmic layer on the cathode layer; and

a cathode metal on the cathode ohmic layer.

5. The apparatus of claim 4, wherein the cathode layer is formed from the group consisting of InP and InAlAs.

6. The apparatus of claim 4, wherein the cathode ohmic layer is formed from the group consisting of InGaAs and InAs.

7. The apparatus of claim 4, wherein the cathode layer is N-doped.

8. The apparatus of claim 4, wherein the cathode layer is P-doped.

9. The apparatus of claim 1, wherein the substrate comprises:

a sub-collector layer;

a collector layer on the sub-collector layer; and

an anode layer on the sub-collector layer.

10. The apparatus of claim 9, wherein the sub-collector layer is formed from the group consisting of InGaAs and InP.

11. The apparatus of claim 9, wherein the collector layer is formed from the group consisting of InGaAs and InP.

12. The apparatus of claim 9, wherein the anode layer is formed from the group consisting of InGaAs and GaAsSb.

13. The apparatus of claim 1, wherein the width W'' and the length L'' of cathode platform is defined by:

$$\frac{J_{AT}(L''-\Delta)(W''-\Delta)}{2J_{PT}(L''+W''-2\Delta)} > 50,$$

with J_{AT} the theoretical unit area current in response to a voltage, C_{AT} the theoretical unit perimeter current in response to the voltage, and Δ the etch bias of the cathode platform.

14. The apparatus of claim 1, further comprising:

a first anode finger spaced adjacent to the first cathode finger;

a second anode finger spaced adjacent to the second cathode finger;

wherein the current between the first anode and first cathode fingers, when a voltage is applied between the fingers, is different than the current between the second anode and second cathode fingers, when the voltage is applied between the second anode and cathode fingers.

15. A testing apparatus in a semiconductor process comprising:

a plurality of interdigitated first cathode fingers and first anode fingers on a substrate each having a first width;

a plurality of interdigitated second cathode fingers and second anode fingers on the substrate each having a second width different than the first width;

wherein either the capacitance between the first cathode and anode fingers is different from the capacitance between second anode and cathode fingers, or the current response to a voltage applied across the first cathode and anode fingers is different from the

current response to the voltage applied across the second anode and cathode fingers.

16. The testing apparatus of claim 15, further comprising:

a cathode bus connecting the plurality of first cathode fingers to a cathode pad; and

an anode bus connecting the plurality of first anode fingers to an anode pad.

17. The testing apparatus of claim 16, further comprising:

cathode measurement means for communicating with the plurality of first cathode fingers; and

anode measurement means for communicating with the plurality of first anode fingers;

wherein either the capacitance or current between the cathode measurement means and anode measurement means is measured.

18. A semiconductor test apparatus, comprising:

a test fixture area occupying a portion of an active area of an integrated circuit; and

a first test fixture in the test fixture area having a plurality of interdigitated first cathode fingers and first anode fingers each with a first width;

a second test fixture in the test fixture area having a plurality of interdigitated second cathode fingers and second anode fingers each with a second width different than the first width;

wherein either the capacitance between the first cathode and anode fingers is different from the capacitance between second anode and cathode fingers, or the current response to a voltage applied across the

first cathode and anode fingers is different from the current response to the voltage applied across the second anode and cathode fingers.

19. The apparatus according to claim 18, further comprising:

pad means for measuring either the capacitance between the first cathode and anode fingers or the current response to a voltage applied across the first cathode and anode fingers.

20. The apparatus according to claim 19, further comprising:

a cathode platform in the test fixture area with a width W'' and length L'' substantially larger than either of the first and second widths.

21. A method of calculating etch bias Δ in a semiconductor-processing step, comprising:

measuring a capacitance between cathode and anode platforms to calculate a unit area capacitance;

measuring a first finger capacitance between a first cathode finger and first anode finger both having a first width;

measuring a second finger capacitance between a second cathode finger and second anode finger both having a second width different than the first width;

calculating the etch bias, Δ, from the unit area capacitance, the first finger capacitance and first finger width, and the second finger capacitance and second finger width.

22. A method according to claim 21, wherein calculating an etch bias, Δ, from the unit area capacitance, the

first finger capacitance and the second finger capacitance further comprises:

performing a linear regression on $C_F(W)$ verses W described by

$$C_F = C_A(L-\Delta)\ (W-\Delta) + 2C_P(L+W-2\Delta)$$

to find $C_F(W=0)$ where C_F is the cathode capacitance of a cathode finger, C_A is the unit area capacitance, L and W are the length and width, respectively, of the first cathode finger, first anode finger, second cathode finger and second anode finger.

23. A method of calculating etch bias Δ in a semiconductor-processing step, comprising:

measuring a current response to a voltage applied across cathode and anode platforms to calculate a unit area current;

measuring a current response to a voltage applied across a first cathode finger and first anode finger both having a first width;

measuring a current response to a voltage applied across a second cathode finger and second anode finger both having a second width different than the first width;

calculating the etch bias, Δ, from the unit area current, the first finger current response and first finger width, and the second finger current response and second finger width.

24. A method according to claim 21, wherein calculating an etch bias, Δ, from the unit area current, the first finger current response and the second finger current response further comprises:

performing a linear regression on $C_F(W)$ verses W described by

$$J_F = J_A(L-\Delta)\ (W-\Delta) + 2J_P(L+W-2\Delta)$$

to find $J_F(W=0)$ where J_F is the cathode current of a cathode finger, J_A is the unit area current, L and W are the length and width, respectively, of the first cathode finger, first anode finger, second cathode finger and second anode finger.